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Structural and electrical analysis of the atomic layer deposition of HfO_2/n-$In_{0.53}Ga_{0.47}As$ capacitors with and without an Al_2O_3 interface control layer

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High mobility III-V substrates with high-*k* oxides are required for device scaling without loss of channel mobility. Interest has focused on the *self-cleaning* effect on selected III-V substrates during atomic layer deposition of Al_2O_3. A thin (~1 nm) Al_2O_3 interface control layer is deposited on $In_{0.53}Ga_{0.47}As$ prior to HfO_2 growth, providing the benefit of *self-cleaning* and improving the interface quality by reducing interface state defect densities by ~50% while maintaining scaling trends. Significant reductions in leakage current density and increased breakdown voltage are found, indicative of a band structure improvement due to the reduction/removal of the $In_{0.53}Ga_{0.47}As$ native oxides. © *2010 American Institute of Physics*. [doi:10.1063/1.3473773]

A critical technological challenge in the integration of high *k*-dielectrics on III-V channels is the control of the high-*k*/III-V interface. Although the interfacial chemistry of the high-*k*/Si system is similar to the SiO_2/Si system,[1] the high-*k*/III-V system is more complex, due to competition between the various native oxide species at the interface,[2] resulting in growth of a poor quality interfacial layer.[3–6] In recent work,[3] reductions in interface state defect densities (D_{it}) were achieved by pre-treatment of the $In_{0.53}Ga_{0.47}As$ surface prior to atomic layer deposition (ALD) of HfO_2 [$k \sim 16–25$, band gap (E_g) ~ 5.8–6.0 eV].[7–9] The native oxides of $In_{0.53}Ga_{0.47}As$ (Ga_2O_3, In_2O_3, and As_2O_3) have low band gaps (3.6–4.8 eV) (Refs. 2 and 9) and *k*-values of 8–10 when relating the reported[9,10] *k*-value for Ga_2O_3 and In_2O_3 with the approximate refractive indices ($n \sim 1.9$ for all)[2] through the equation $n^2 \propto k$ and the Moss Inverse Law[11] for the refractive index, *k*-value and energy band gap. They are detrimental to the band structure of high-*k*/III-V devices by increasing the leakage current and creating potential wells in the native oxide layer between the high-*k* oxide and the substrate. The *self-cleaning* Al_2O_3 ALD process is reported to reduce or remove the III-V native oxides.[12–15] However, devices employing Al_2O_3 ($k \sim 8.6–11.6$, $E_g \sim 8.8$ eV) (Refs. 8, 9, and 12) as the gate oxide are limited for scaling due to its low *k*-value.

In this work, the structural and electrical properties of Pd/HfO_2/*n*-$In_{0.53}Ga_{0.47}As$ devices (HfO_2: nominal thickness ~3, ~4, and ~5 nm) with/without an ~1 nm Al_2O_3 interface control layer (ICL), are examined using high resolution transmission electron microscopy (HR-TEM) and current/capacitance/conductance versus voltage measurements (JV, CV, and GV, respectively). The devices are labeled: *s*1_3, *s*1_4, *s*1_5 (e.g., sample, ~1 nm Al_2O_3, ~5 nm HfO_2 is labeled *s*1_5). As a control, devices were fabricated without the Al_2O_3 ICL [nominal ~5 nm HfO_2 only (label: *s*0_5)]. The motivation for this work is: (i) to detect any improvement in the quality and structure of the interface using the bilayer approach; (ii) to investigate if an Al_2O_3 ICL improves the electrical performance of devices by modifying the metal-oxide-semiconductor (MOS) band structure; (iii) to determine if scaling is possible with an Al_2O_3 ICL using reducing thicknesses of HfO_2.

The ~2 μm *n*-type (S: $\sim 4 \times 10^{17}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ channels had a ~0.1 μm InP buffer layer (S: $\sim 2 \times 10^{18}$ cm^{-3}) on a ~350 μm InP substrate (S: $3–8 \times 10^{18}$ cm^{-3}). All $In_{0.53}Ga_{0.47}As$ layers were grown by MOVPE. An *ex situ* three-stage surface pre-treatment process [HCl, NH_4OH, and $(NH_4)_2S$] was performed on the *n*-$In_{0.53}Ga_{0.47}As$/InP substrates which has previously been shown to be beneficial to device performance.[3] The Al_2O_3 and HfO_2 layers were deposited in a Cambridge NanoTech Fiji F200LLC ALD system, at 250 °C. The ALD of Al_2O_3 and HfO_2 employed alternating pulses of TMA [$Al(CH_3)_3$]/H_2O and tetrakis(ethylmethylamino)hafnium (TEMAH) {$Hf[N(C_2H_5)(CH_3)]_4$}/H_2O, respectively. MOS structures were completed by vacuum evaporation of ~200 nm of Pd at a deposition rate of 2.5 Å/s using a lift-off process. No ohmic back contacts were formed.

Figures 1(a) and 1(b) present cross-sectional HR-TEM micrographs of *s*1_5 and *s*0_5, confirming the physical oxide and nominal thicknesses are in close agreement: *s*1_5 [Fig. 1(a)] has a ~5.3 nm HfO_2 layer, and a ~1.2 nm Al_2O_3 layer. *s*0_5 [Fig. 1(b)], has a ~4.9 nm HfO_2 layer. All oxide layers are amorphous. Comparison between Figs. 1(a) and 1(b) shows a ~0.7 nm native oxide layer at the high-*k*/*n*-$In_{0.53}Ga_{0.47}As$ interface when no Al_2O_3 ICL is deposited, which is indicative of an Al_2O_3 *self-cleaning* effect on the native oxide, for sample *s*1_5.

Figure 2(a) presents a cross-sectional HR-TEM micrograph of *s*1_3. The physical thicknesses of HfO_2 and Al_2O_3 are ~3.2 nm and ~1.2 nm, respectively. Figure 2(b), a plan-view HR-TEM micrograph for sample *s*1_5, reveals the epitaxial 2 μm *n*-$In_{0.53}Ga_{0.47}As$ layer to be defect-free,

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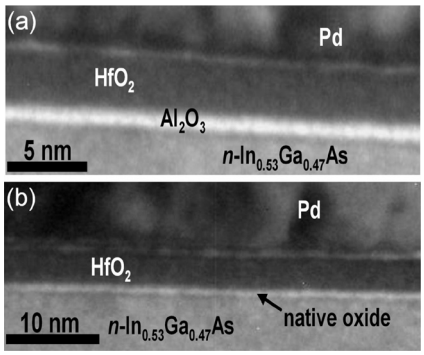

FIG. 1. Cross-sectional HR-TEM micrographs of (a) *s*1_5, with ~5.3 nm HfO_2 and ~1.1 nm Al_2O_3 and (b) *s*0_5, with ~4.9 nm HfO_2 and a ~0.7 nm native oxide layer.

with an associated negligible root mean square (rms) surface roughness of <1 nm.

Figure 3 shows (a) JV responses and (b) the measured 1 kHz CV responses, along with the simulated[16] CV curves for all samples. The inset to Fig. 3(a) shows the capacitance equivalent thickness (CET) versus HR-TEM extracted HfO_2 physical thickness plot for the bilayer sample set (*s*1_3,*s*1_4,*s*1_5), with a linear fit. Figure 3(a), when assessing the bilayer sample set only, shows that leakage current density increases with reducing HfO_2 thickness, and the dielectric breakdown voltage increases with increasing HfO_2 thickness. This is expected for a dominant quantum-mechanical (QM) tunneling leakage mechanism with similar energy barrier height and shape, and for a dominant electrically-controlled oxide breakdown process.[17] However, the leakage current density response for sample *s*0_5 is substantially higher (approximately three orders of magnitude at 3 V) than for sample *s*1_5, showing that the absence of an Al_2O_3 ICL changes the tunneling barrier height/shape to conduction beyond a thickness-dependency regime only and introduces an additional, highly temperature-dependent (not shown), trap-assisted conduction mechanism that adds magnitude and fluctuation to the response.[18] Figure 3(b) shows that the accumulation maximum capacitance at 2 V scales correctly with oxide thickness for the bilayer sample set. The simulated curves confirm that surface accumulation is achieved at 2 V for all samples.[3] The accumulation maximum capacitance is greater for the measured data compared to the simulated data, showing the existence of a QM correction factor. This difference could be due to additional states inside the conduction band at the oxide/n-$In_{0.53}Ga_{0.47}As$ interface,[19] and/or charge quantization leading to X and L satellite valley occupation in the conduction band.[20] We see a similar maximum accumulation capacitance for the ~5 nm HfO_2 samples with/without Al_2O_3 (*s*1_5 and *s*0_5, respectively), showing that the overall equivalent oxide thickness of these oxide stacks are similar. The observed variation in the maximum accumulation capacitance (~0.003 F/m^2) for sample *s*0_5 is likely due to native oxide layer thickness variation not observable by HR-TEM. Given the large difference in leakage current density between these samples (*s*1_5 and *s*0_5), it is evident that the Al_2O_3 ICL substantially reduces the native oxide layer thickness while increasing the barrier height to electron tunneling from the $In_{0.53}Ga_{0.47}As$ conduction band. The linear fit of the inset to Fig. 3(a) shows that the reduction in HfO_2 thickness for the bilayer structures produces the required scaling trend. This linear fit can be used to extract an intercept CET value, which has contributions from Al_2O_3, any underlying native oxide layer (if present), and the QM correction contribution from the n-$In_{0.53}Ga_{0.47}As$ accumulation layer. HR-TEM [Figs. 1(a), 1(b), and 2(a)], in combination with the electrical results [Figs. 3(a), 3(b), 4(a), and 4(b)], indicate that no substantive underlying native oxide layer is present for the bilayer sample set. Assuming this is the case and since we can extract the contributions from Al_2O_3, we can thereby determine a QM correction factor of ~0.7 nm. From the slope of the linear fit we can estimate the HfO_2 k-value to be ~20, which is within the reported range.[7] Reasonable assumptions used were: (i) the k-value of both Al_2O_3 and any native oxide[2,10,12] layer is ~9 and (ii) the physical thicknesses used for sample *s*1_4 are nominal thicknesses proportionally corrected using HR-TEM/nominal-thickness ratios and ALD cycle ratios for other samples. The absence of an underlying native oxide

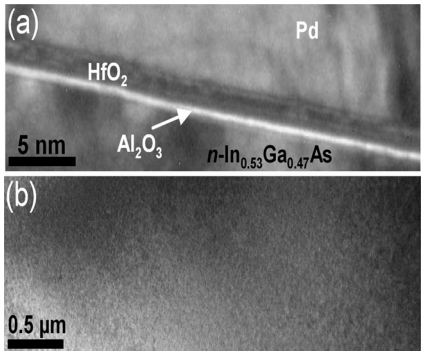

FIG. 2. HR-TEM micrographs of (a) *s*1_3 (cross-sectional), with ~3.2 nm HfO_2 and ~1.2 nm Al_2O_3; (b) *s*1_5 (plan-view) shows a defect free n-$In_{0.53}Ga_{0.47}As$ substrate layer.

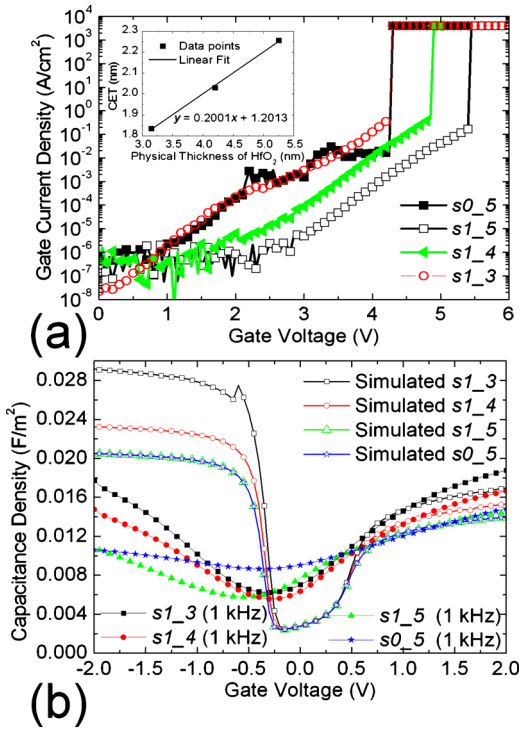

FIG. 3. (Color online) (a) JV responses for all samples, with significantly lower leakage for the *s*1_5 (Al_2O_3 ICL) devices, compared to *s*0_5 devices. (b) Measured and simulated (from the 1D Poisson–Schrödinger solver) 1 kHz CV responses for all samples. Inset to (a) shows the CET vs physical thickness with a linear fit.

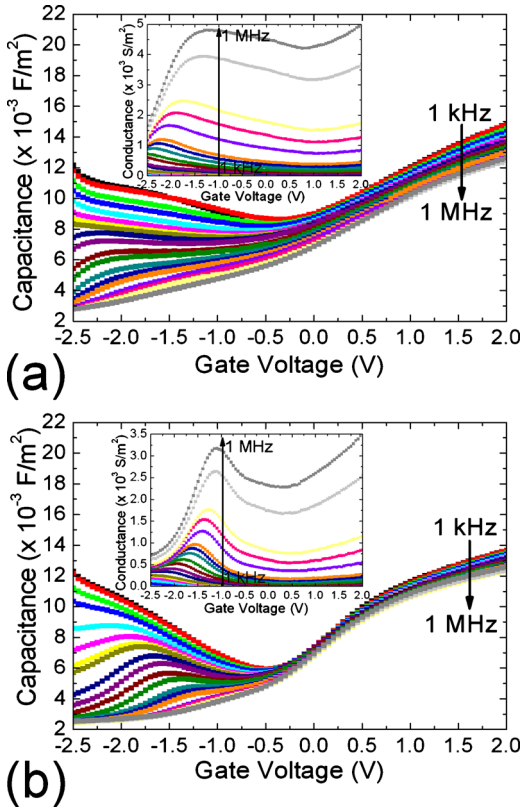

FIG. 4. (Color online) (a) and (b) show CV responses (20 frequencies; 1 kHz–1 MHz) for samples *s*0_5 and *s*1_5, respectively. The insets to (a) and (b) show the corresponding GV responses.

layer, evidenced by HR-TEM in combination with the electrical results, indicates that the Al_2O_3 is likely to be removing the native oxides via the *self-cleaning* process.

Figures 4(a) and 4(b) show the multifrequency CV responses for samples *s*0_5 and *s*1_5, respectively. The insets to Figs. 4(a) and 4(b) show the corresponding GV responses. We observe an increased D_{it} response in both the CV and GV profiles for sample *s*0_5 when compared to the equivalent response for sample *s*1_5, which includes (over the entire voltage range) an increased CV and GV stretch-out and frequency dispersion. In the voltage range −1 to 0.25 V, the absence of minority carriers is assumed, corresponding to the depletion regime. An approximation to the Conductance Method[21] indicates that samples *s*0_5 and *s*1_5 have estimated D_{it} values of $\sim 8\times10^{12}$ $cm^{-2}\,eV^{-1}$ and $\sim 4\times10^{12}$ $cm^{-2}\,eV^{-1}$, respectively. Due to the absence of distinct equivalent parallel conductance (G_p/ω) peaks as observed in SiO_2/Si systems, this is derived assuming zero standard deviation in band bending using values of G_p/ω at −1 V and taken at 30 kHz. While it is noted that the G_p/ω magnitudes may be affected by the approximation conditions, and any possible minority carrier contribution, the relative difference provides a valid estimate. There is approximately a 50% reduction in D_{it} when including an Al_2O_3 ICL.

In summary, it is found that the inclusion of a thin Al_2O_3 ICL (~1 nm) at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface improves the structural and electrical properties of $Pd/HfO_2/n\text{-}In_{0.53}Ga_{0.47}As$ devices. The inclusion of the Al_2O_3 ICL improves the breakdown voltage and reduces leakage current densities by approximately three orders of magnitude at 3 V by increasing the barrier height to tunneling from the $In_{0.53}Ga_{0.47}As$ conduction band into the oxide. No apparent native oxide layer is observed at the high-$k/In_{0.53}Ga_{0.47}As$ interface when using an Al_2O_3 ICL, suggesting that the Al_2O_3 ALD process is *self-cleaning* the $In_{0.53}Ga_{0.47}As$ native oxides. Comparing the electrical performance for the bilayer samples with different HfO_2 thicknesses we find that device scaling trends can be achieved. Combining the structural and electrical results we find a QM correction factor of ~0.7 nm. The inclusion of an ICL causes an approximate 50% reduction in D_{it}, thereby improving the quality of the interface.

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[1]P. K. Hurley, K. Cherkaoui, É. O'Connor, M. C. Lemme, H. D. B. Gottlob, M. Schmidt, S. Hall, Y. Lu, O. Buiu, B. Raeissi, J. Piscator, O. Engstrom, and S. B. Newcomb, J. Electrochem. Soc. **155**, G13 (2008).
[2]C. W. Wilmsen, *Physics and Chemistry of III-V Compound Semiconductor Interfaces* (Plenum, New York, 1985).
[3]É. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, and P. K. Hurley, Appl. Phys. Lett. **94**, 102902 (2009).
[4]N. Goel, P. Majhi, C. O. Chui, W. Tsai, D. Choi, and J. S. Harris, Appl. Phys. Lett. **89**, 163517 (2006).
[5]É. O'Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, P. K. Hurley, B. Brennan, G. Hughes, and S. B. Newcomb, Appl. Phys. Lett. **92**, 022902 (2008).
[6]W. Tsai, N. Goel, S. Koveshnikov, P. Majhi, and W. Wang, Microelectron. Eng. **86**, 1540 (2009).
[7]K. Kukli, J. Niinistö, A. Tamm, J. Lu, M. Ritala, M. Leskelä, M. Putkonen, L. Niinistö, F. Song, P. Williams, and P. N. Heys, Microelectron. Eng. **84**, 2010 (2007).
[8]J. Robertson and B. Falabretti, Mater. Sci. Eng., B **135**, 267 (2006).
[9]D. P. Norton, Mater. Sci. Eng. R. **43**, 139 (2004).
[10]M. Passlack, R. Droopad, P. Fejes, and L. Wang, IEEE Electron Device Lett. **30**, 2 (2009).
[11]T. S. Moss, Proc. Phys. Soc. London, Sect. B **63**, 167 (1950).
[12]P. D. Ye, G. D. Wilk, B. Yang J. Kwo, S. N. G. Chu, S. Nakahara, H.-J. L. Gossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude, Appl. Phys. Lett. **83**, 180 (2003).
[13]M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Miller, Appl. Phys. Lett. **86**, 152904 (2005).
[14]C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, Appl. Phys. Lett. **92**, 071901 (2008).
[15]B. Brennan, M. Milojevic, H. C. Kim, P. K. Hurley, J. Kim, G. Hughes, and R. M. Wallace, Electrochem. Solid-State Lett. **12**, H205 (2009).
[16]Professor G. Snider, University of Notre Dame, one-dimensional (1D) Poisson–Schrödinger solver, parameters used with HR-TEM oxide thicknesses; Al_2O_3:k=9, E_g=8.8 eV, ΔE_c=3.45 eV; HfO_2:k=20, E_g=6.0 eV, and ΔE_c=2.25 eV; $In_{0.53}Ga_{0.47}As$ native oxide: k=9, E_g=4.1 eV, ΔE_c=1.5 eV. InP/$In_{0.53}Ga_{0.47}As$ thickness/doping as specified. Temperature=300 K.
[17]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981).
[18]F. Crupi, G. Giusi, G. Iannaccone, P. Magnone, C. Pace, E. Simoen, and C. Claeys, J. Appl. Phys. **106**, 073710 (2009).
[19]G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, Appl. Phys. Lett. **95**, 202109 (2009).
[20]T. P. O'Regan, P. K. Hurley, B. Sorée, and M. V. Fischetti, Appl. Phys. Lett. **96**, 213514 (2010).
[21]E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982).